[Delay Lock Circuit Using Bisection Algorithm and Related Method]

Abstract of Disclosure

A method for performing a delay lock to generate a second clock according to a first clock and to synchronize the second clock with the first clock is provided. The method has correcting processes executed to increase or decrease, by a correction interval, a delay time between corresponding periods of the first clock and the second clock. The correction interval for a subsequent correcting process is substantially half the previous correction interval of the previous correcting process.

Figures